

Cryostat – Detector FrontEnd Electronics Electrical Interface

Interface Document: LN-MPIA-FDR-INT-211		Issue: 1.2
Relevant Documents: LN-MPIA-FDR-ELEC-001, LN-MPIA-TN-ELEC-001		
Brief Description: Electrical Interface between the Detector FrontEnd Electronics and the Cryostat		
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Interface Description

This document describes the electrical interface between the detector frontend electronics and the cryostat. The clocks, biases and the video signals have their connectors on the outside of the cryostat.

Interface Specification

The four connectors on the cryostat are specified in the following tables, :

Bias Connector

PTIH06SE16-26P	signal
A	Dsub
B	GND
C	GND
D	VDDA
E	VLOAD2
F	GND
G	GND
H	ext bias
J	GND
K	GND
L	+VCC
M	+VCC
N	Biasgate
P	Drain
R	GND
S	GND
T	VLOAD3
U	GND
V	GND
W	VReset
X	Biaspower
Y	VLOAD1
Z	VLOAD4
a	-VCC
b	-VCC
c	VDD

Clock Connector

PTIH06SE18-32P	signal
B	Clk1
L	Clk2
F	ClkB1
C	ClkB2
G	Fsync
K	Lsync
E	Velk
D	Reset
N	Read
J	Lrst
X	O1
Y	O2
H	Reset
Z	Clkd Dr.
P	clk cla
A	GND

Video Connector 1

PTIH 22-55P	signal
A	Video GND
B	PRE GND
C	Schirm
D	Sig+1
E	Sig-1
F	Sig+2
G	Sig-2
H	Sig+3
J	Sig-3
K	Sig+4
L	Sig-4
M	Sig+5
N	Sig-5
P	Sig+6
R	Sig-6
S	Sig+7
T	Sig-7
U	Sig+8
V	Sig-8
W	Sig+9
X	Sig-9
Y	Sig+10
Z	Sig-10
a	Sig+11
b	Sig-11
c	Sig+33
d	Sig-33
e	Sig+34
f	Sig-34
g	Sig+35
h	Sig-35
i	Sig+36
j	Sig-36

Video Connector 2

PTIH 24-61P	signal name
A	Video GND
B	PRE GND
C	Schirm
D	Sig+12
E	Sig-12
F	Sig+13
G	Sig-13
H	Sig+14
J	Sig-14
K	Sig+15
L	Sig-15
M	Sig+16
N	Sig-16
P	Sig+17
R	Sig-17
S	Sig+18
T	Sig-18
U	Sig+19
V	Sig-19
W	Sig+20
X	Sig-20
Y	Sig+21
Z	Sig-21
a	Sig+22
b	Sig-22
c	Sig+23
d	Sig-23
e	Sig+24
f	Sig-24
g	Sig+25
h	Sig-25
i	Sig+26
j	Sig-26
k	Sig+27
m	Sig-27
n	Sig+28
p	Sig-28
q	Sig+29
r	Sig-29
s	Sig+30
t	Sig-30
u	Sig+31
v	Sig-31
w	Sig+32
x	Sig-32

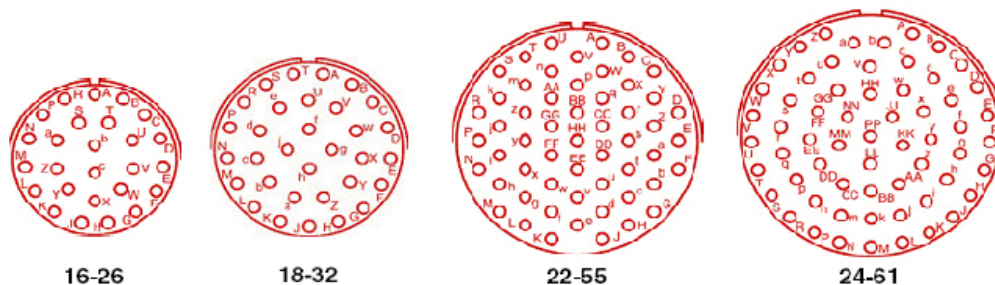


Figure 1: Bias, clock and video signal connectors

Special Requirements

Handle with care.